### CSE460: VLSI Design

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Section- 07

Lab Assignment 3

Question 1:

Write Verilog code for 1001 or 1111 pattern detector both

1. as a Moore type FSM and
2. as a Meal type FSM.

So, for each type of FSM, your report must contain the following:

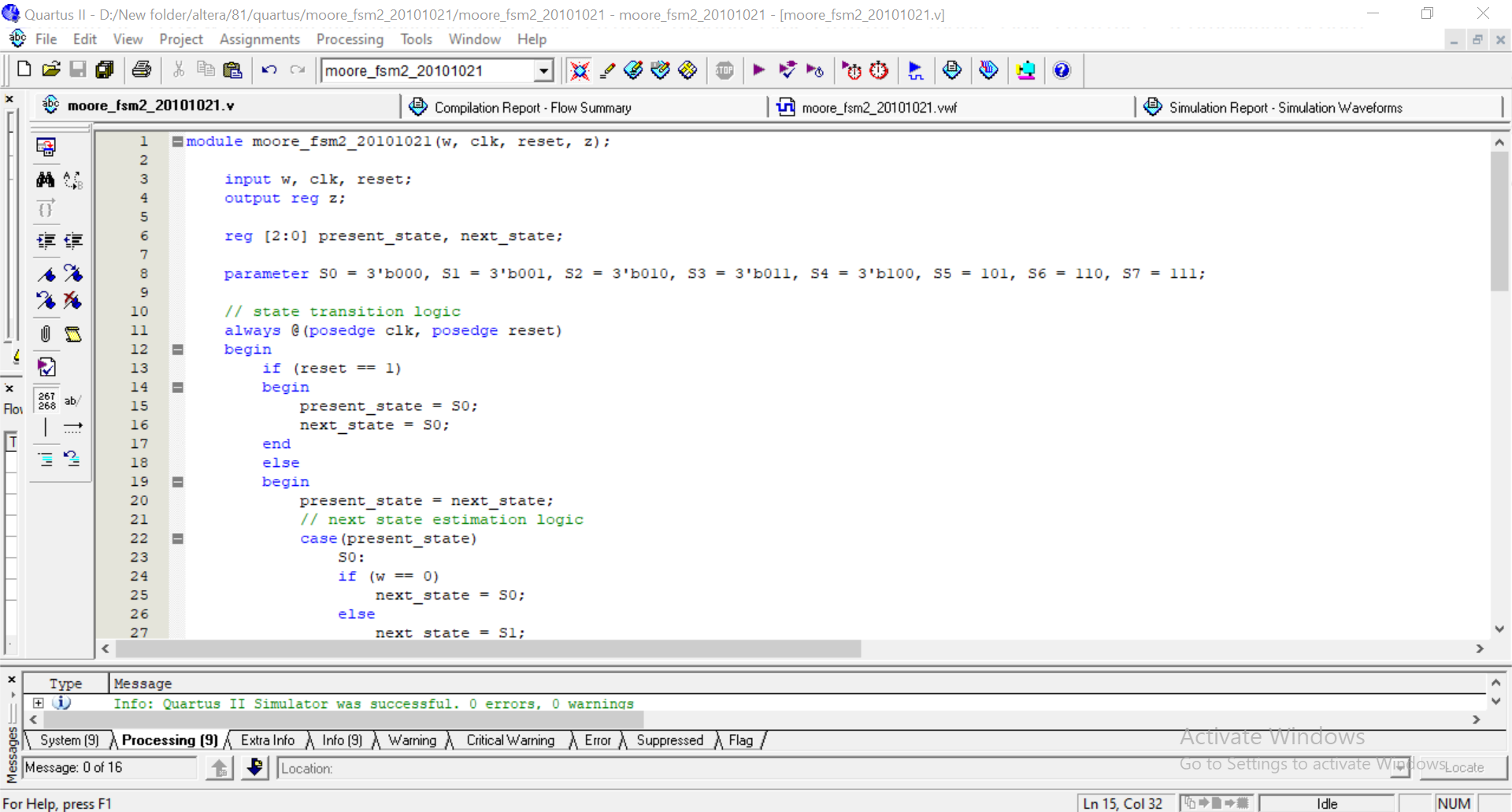
1. Screenshot of the Verilog Code
2. Screenshot of the timing diagram showing the patterns are detected successfully
3. Discussion and comments on the timing diagram.

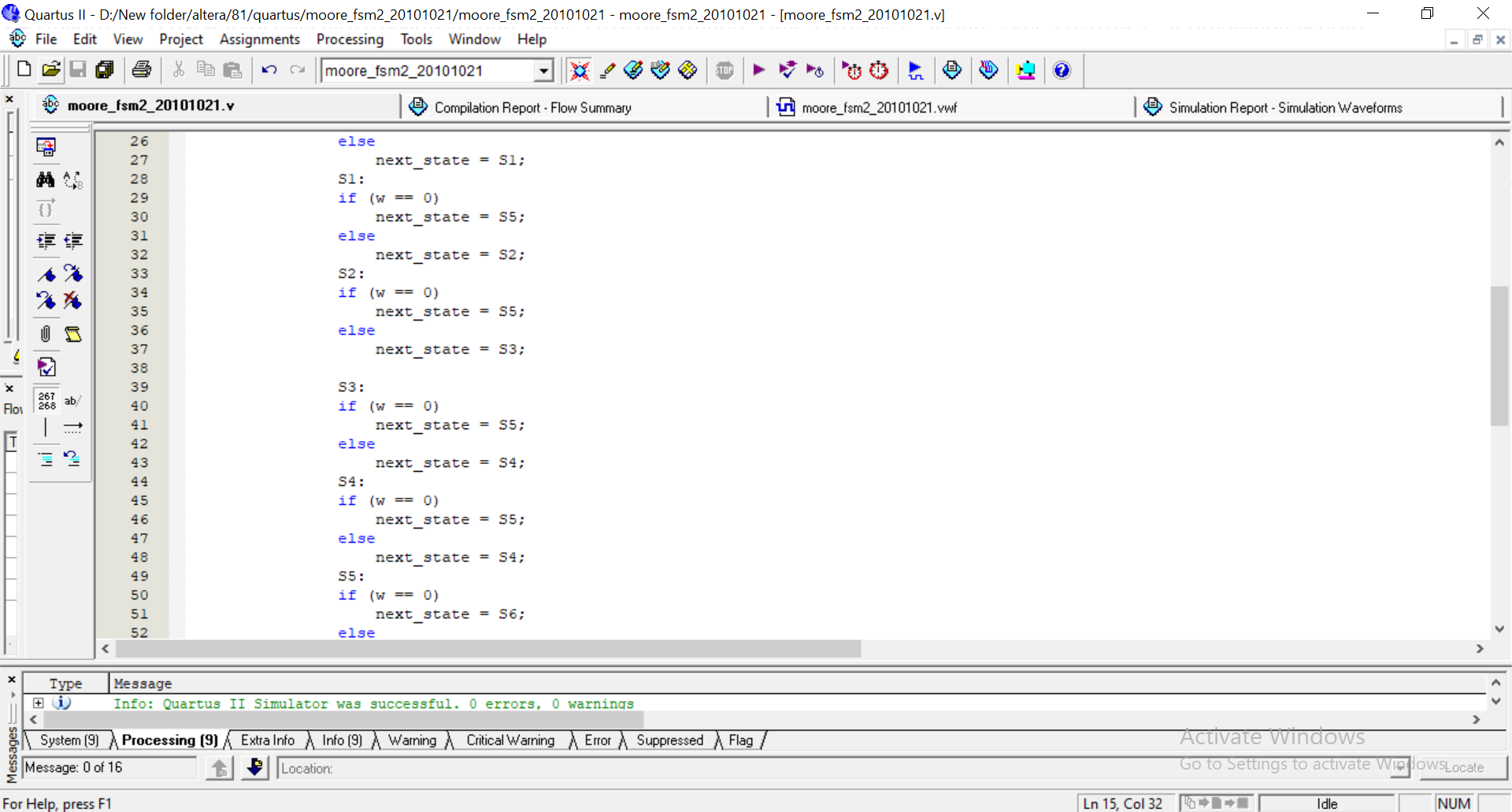
[State Diagram are provided in the slide]

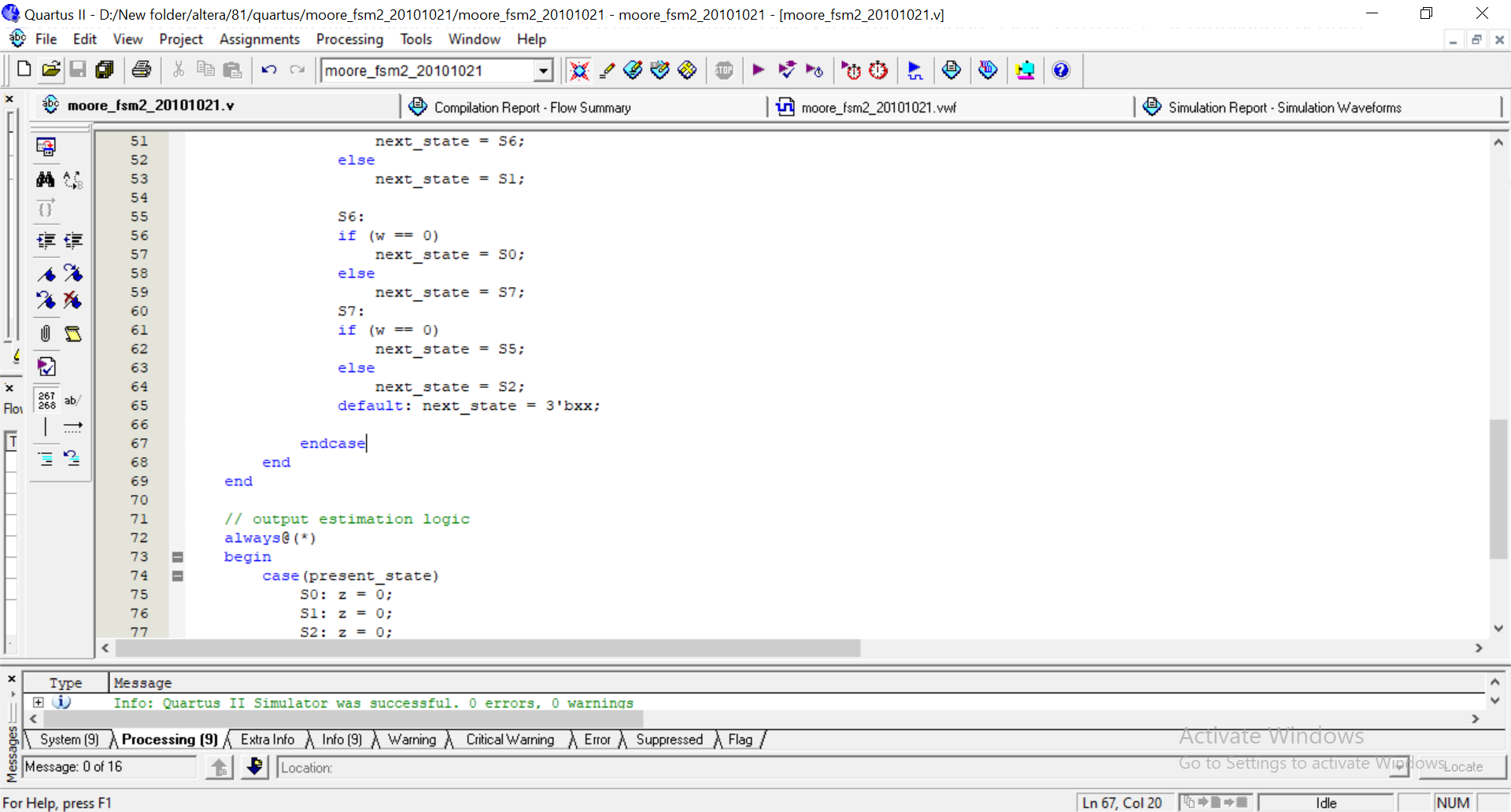
Answer:

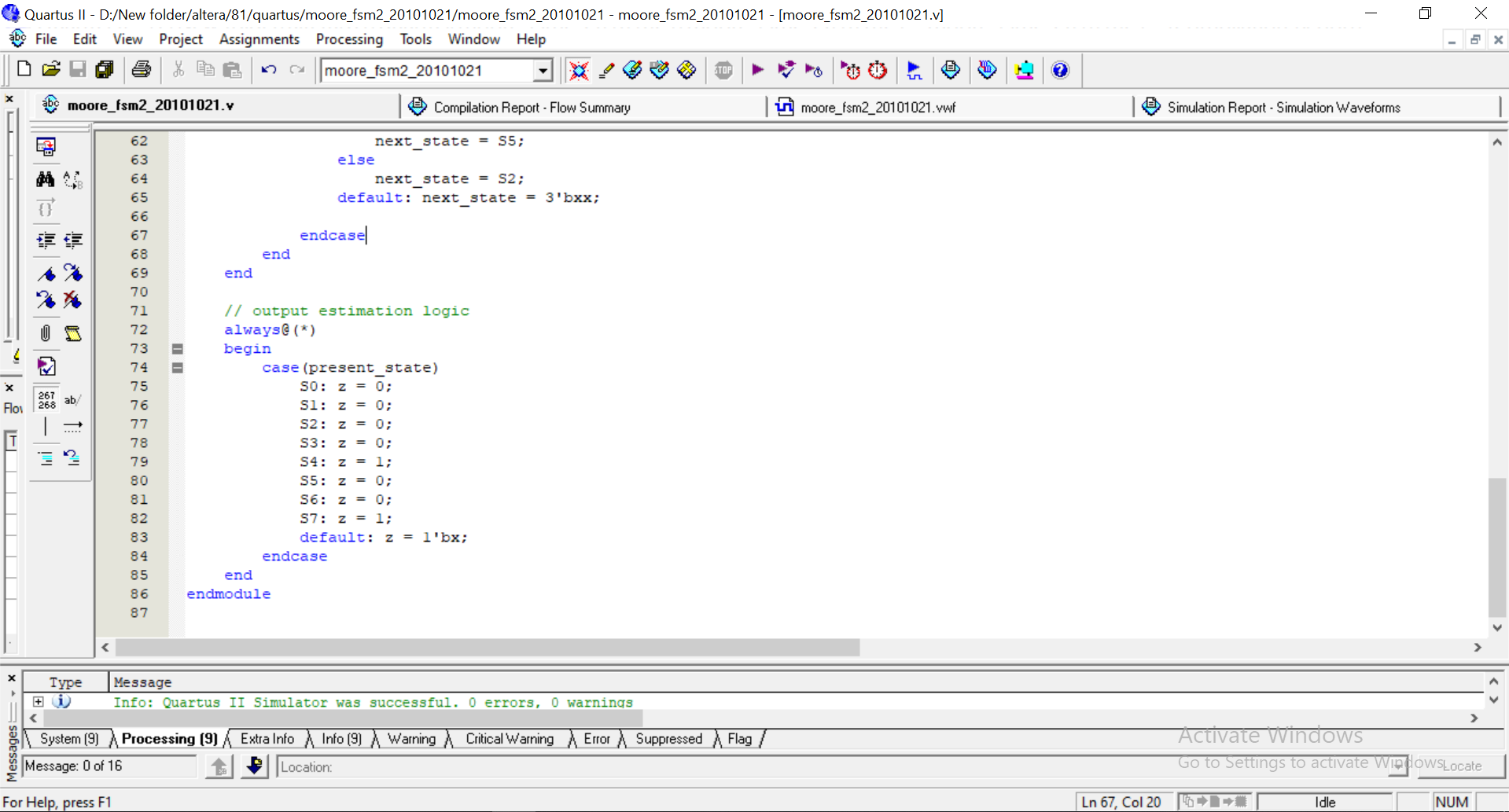
# **Problem 1(a) – Moore FSM:**

1. **Screenshot of the Verilog Code**

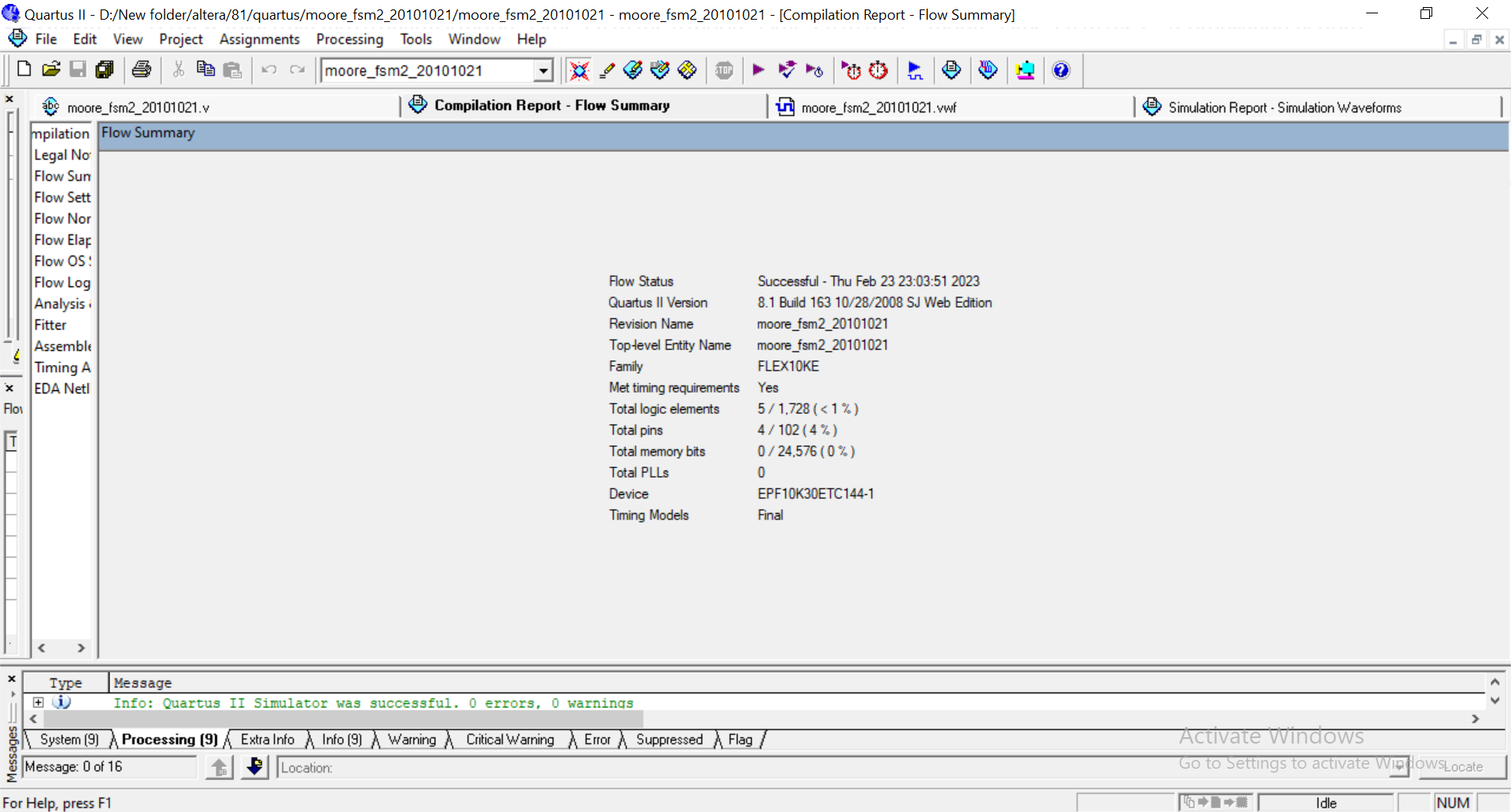
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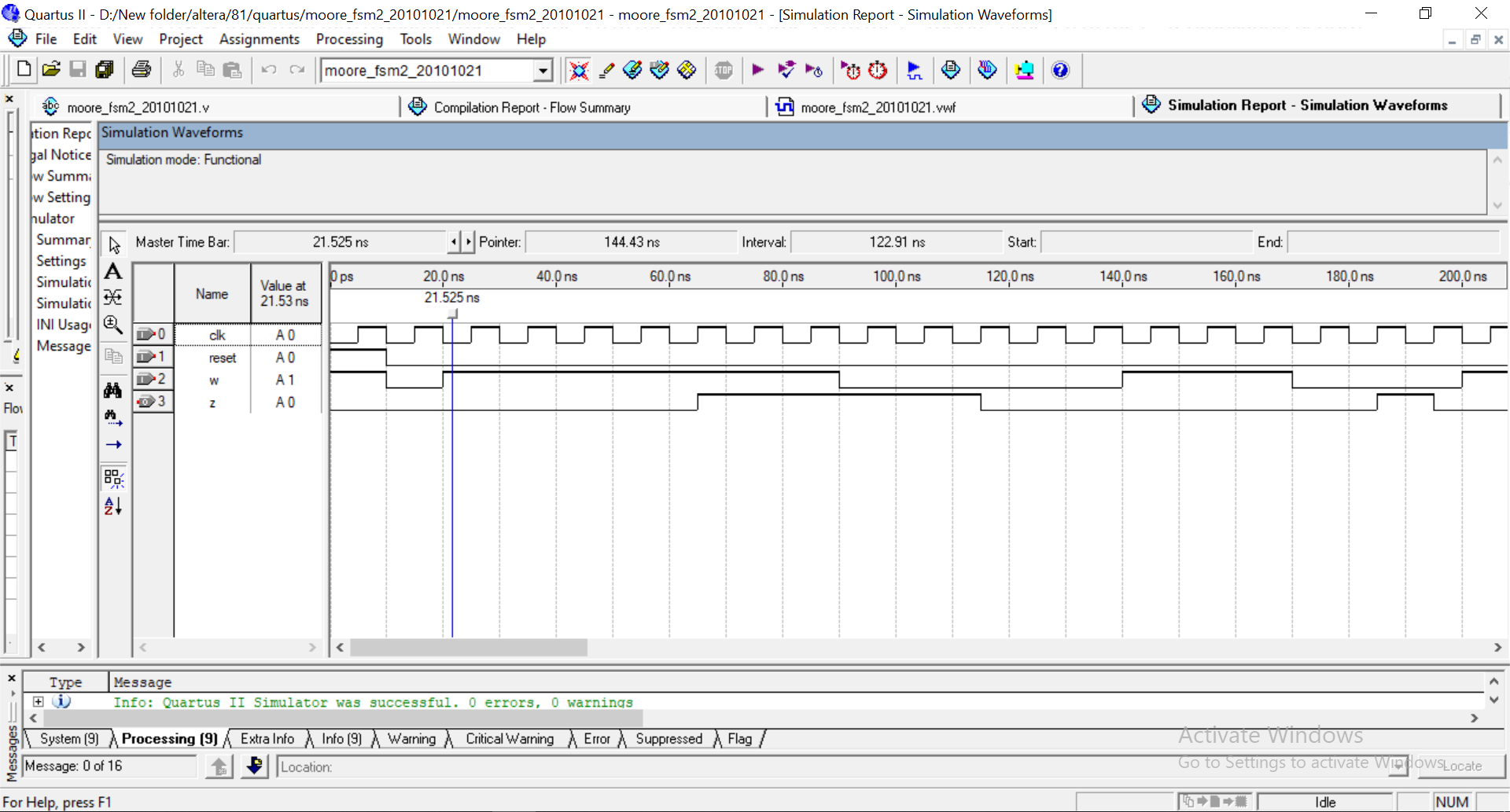
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**Compilation Report:**

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1. **Screenshot of the timing diagram showing the patterns are detected successfully**



1. **Discussion and comments on the timing diagram.**

We know, in Moore type FSM, output of the sequential circuit depends only on the states of the circuit.

And since the above code shows this characteristic, it is a Moore type FSM.

Here, the finite state machine generates output, z =0 when the previous 4 values of w were 1001 or 1111; otherwise output low, z=0, is returned.

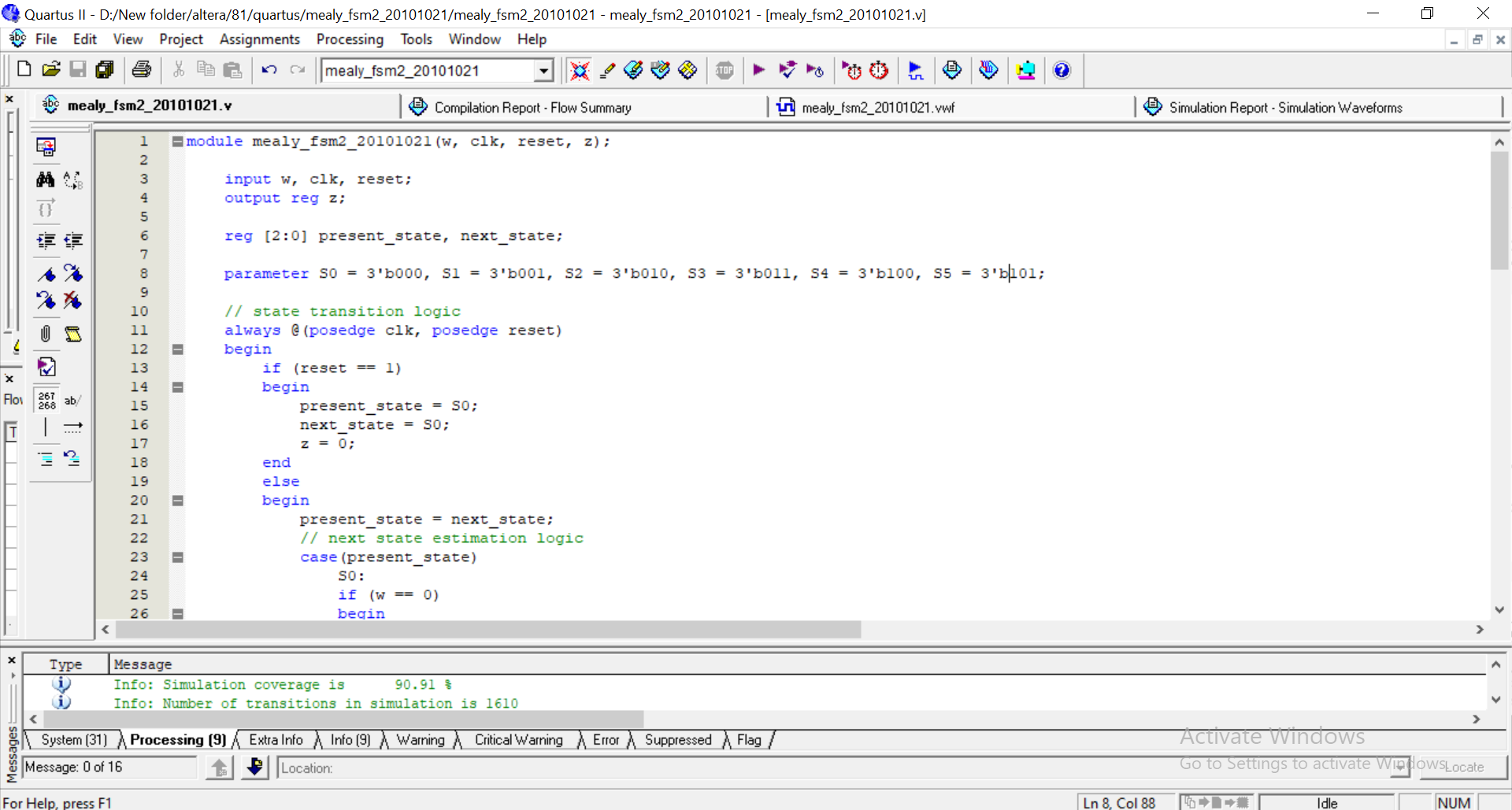
At the beginning of the code, initial state is set as S0 where reset =1 as the Moore State Diagram suggests.

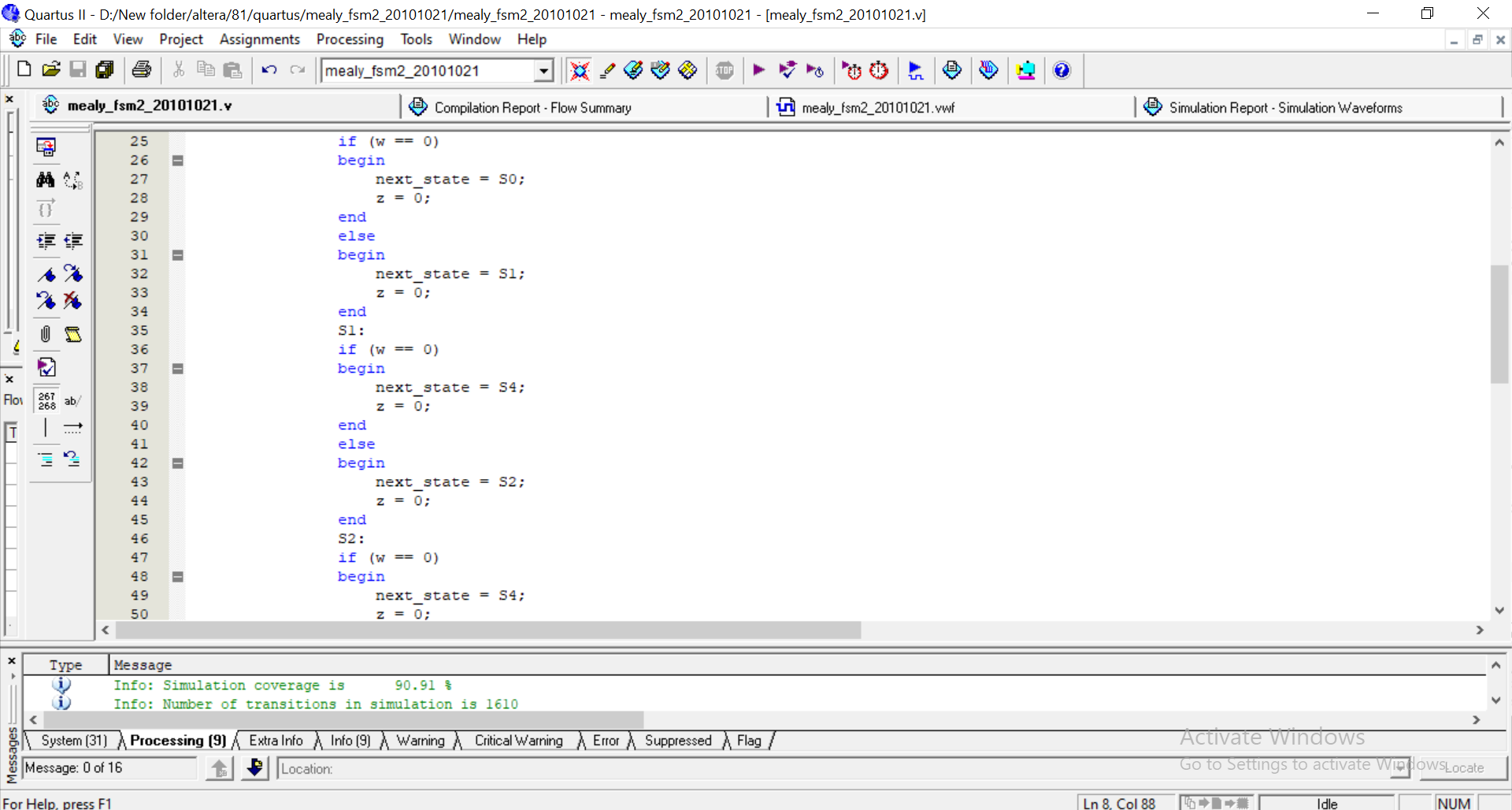
For reset = 0, the conditions for the state table are applied for randomized values of w.

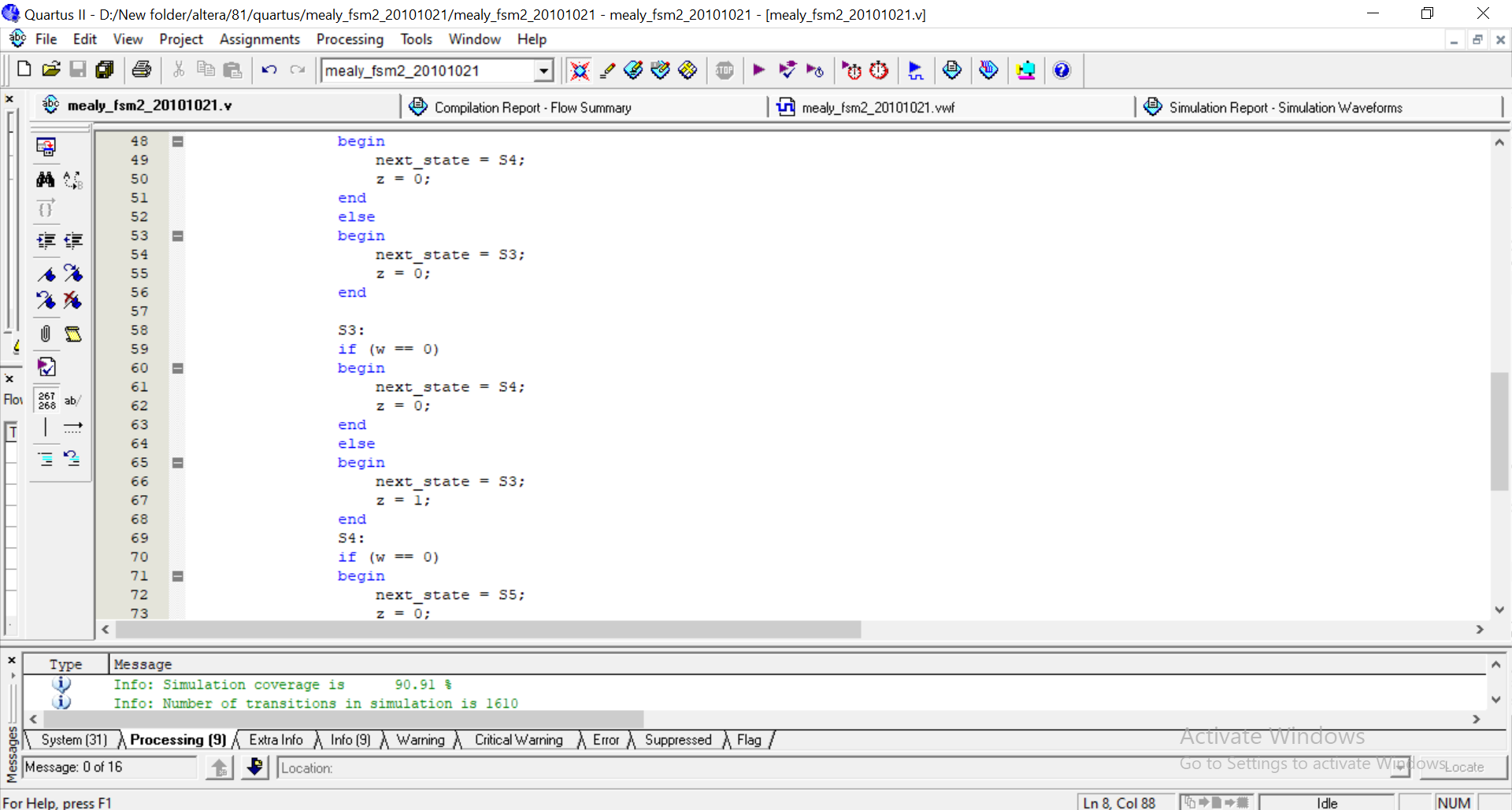
We can see from the simulation that for each 1001 or 1111 pattern detected in w values, at 4 consecutive positive edges of clock, after that, a positive-edged output, z=1, is noticed and hold till the following positive edge.

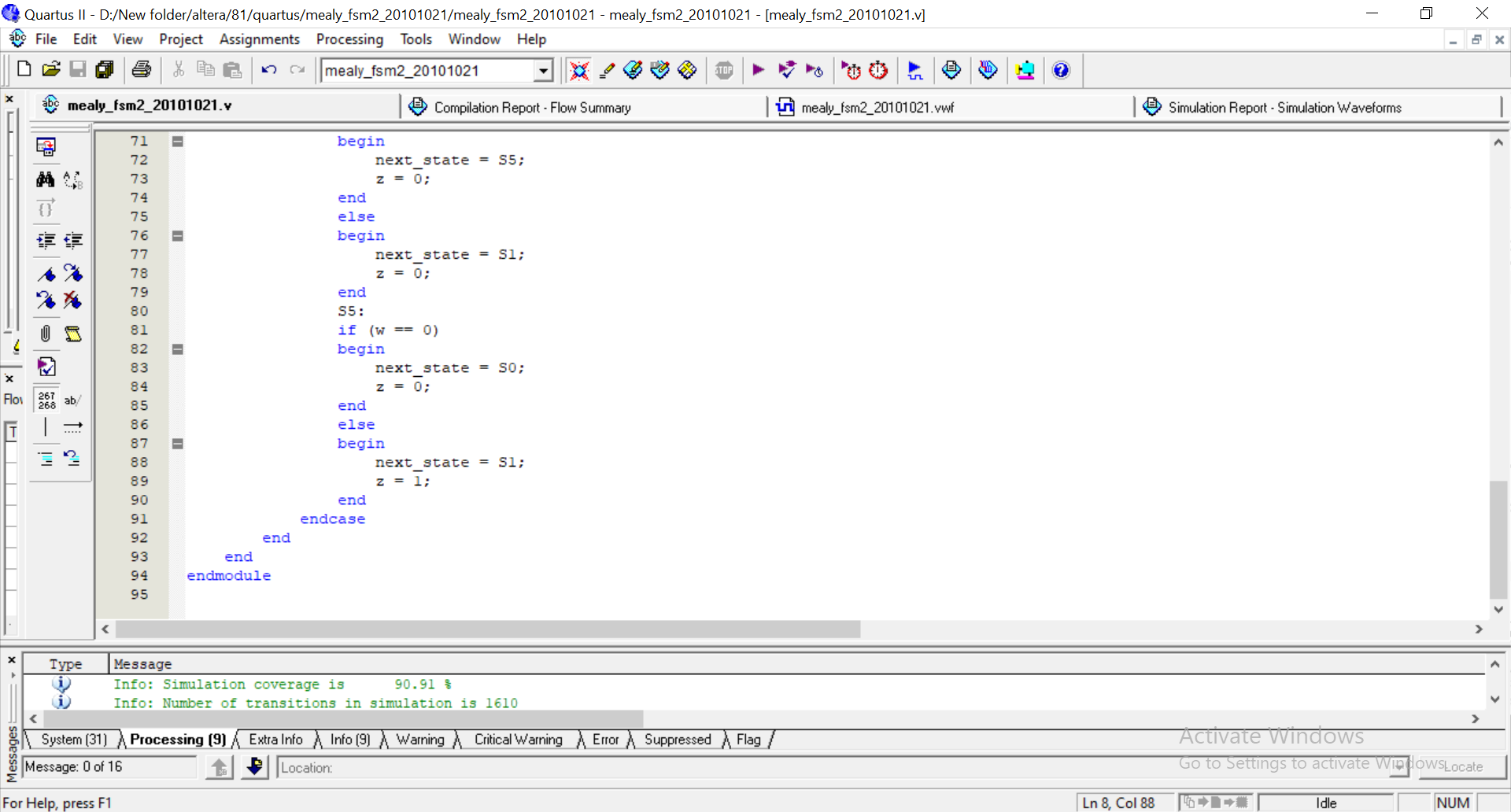
# **Problem 1(b) – Mealy FSM:**

1. **Screenshot of the Verilog Code**

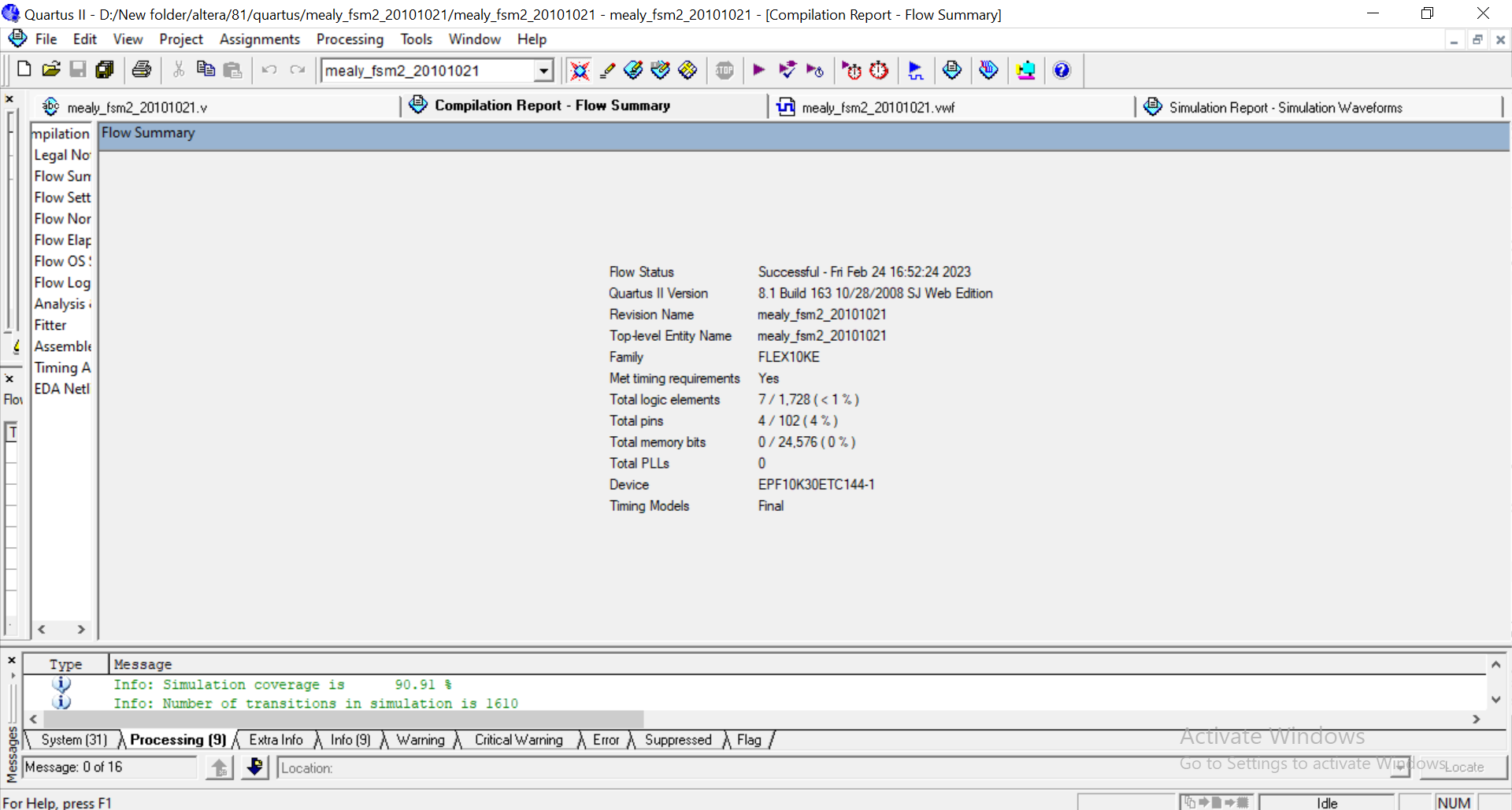
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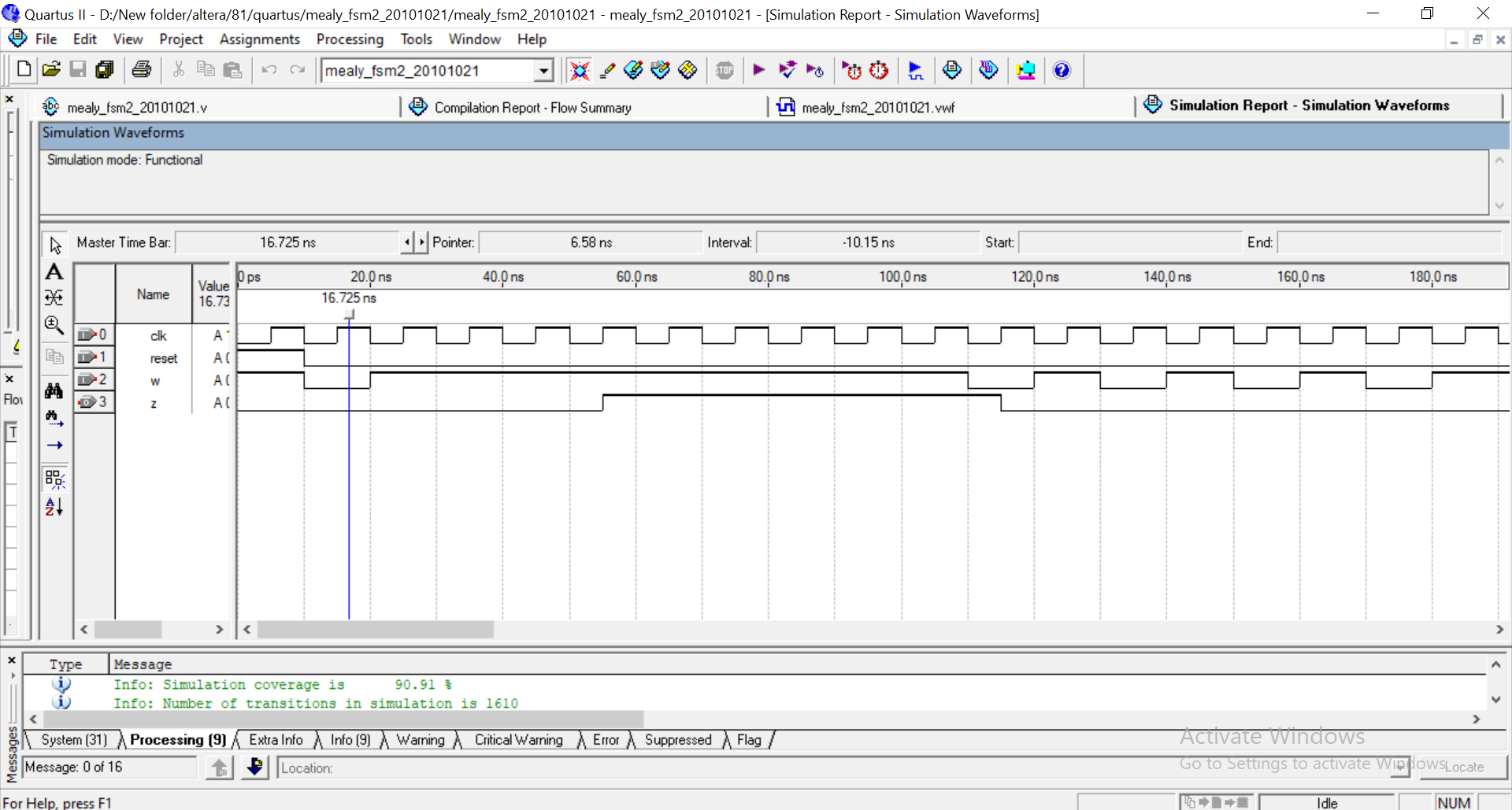
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**Compilation Report:**

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1. **Screenshot of the timing diagram showing the patterns are detected successfully**

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1. **Discussion and comments on the timing diagram.**

We know, in Mealy type FSM, output of the sequential circuit depends on the states of the circuit and the present values of its input.

And since the above code shows this characteristic, it is a Moore type FSM.

Here, the finite state machine generates output, z =0 when the previous 4 values of w were are 1001 or 1111; otherwise output low, z=0, is returned.

At the beginning of the code, initial state is set as S0 where reset =1 as the Mealy State Diagram suggests.

For reset = 0, the conditions for the state table are applied for randomized values of w.

Mealy type needs smaller number of states in comparison to Moore type FSM. We can see from the simulation that the FSM successfully recognizes the patterns and returns the desired output for z.